



High Speed CMOS TTL Input – 54HCT04

Hex Inverter Logic IC with LSTTL compatible inputs in bare die form

Rev 2.0
18/08/25

Description

The 54HCT04 Hex Inverter is fabricated using a small feature size CMOS process that combines high speed LSTTL performance with CMOS low power. The device is commonly used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs and contains six independent inverters with standard push-pull outputs which perform the Boolean function $Y = \bar{A}$ in positive logic. All inputs are protected against ESD and excess voltage transients. Device inputs directly accept LSTTL or CMOS.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 4.5V to 5.5V
- TTL / CMOS compatible Input Levels
- Function compatible with 54LS04
- Full Military Temperature range.

Ordering Information

The following part suffixes apply:

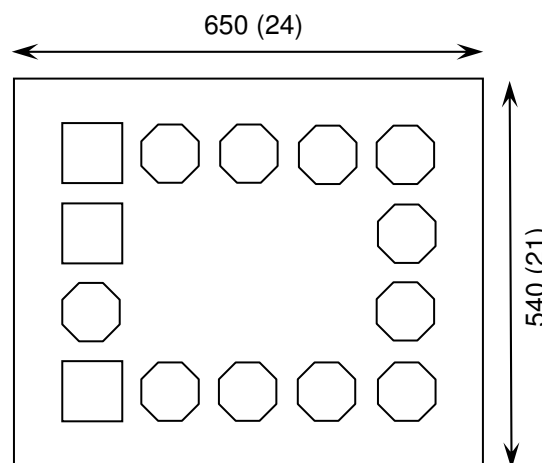
- No suffix - MIL-STD-883 /2010B Visual Inspection
- “H” - MIL-STD-883 /2010B Visual Inspection
+ MIL-PRF-38534 Class H LAT
- “K” - MIL-STD-883 /2010A Visual Inspection (Space)
+ MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	650 x 540 24 x 21	µm mils
Minimum Bond Pad Size	76 x 76 3 x 3	µm mils
Die Thickness	280 (±20) 11.02 (±0.79)	µm mils
Top Metal Composition	Al/Si/Cu	
Back Metal Composition	N/A – Bare Si	

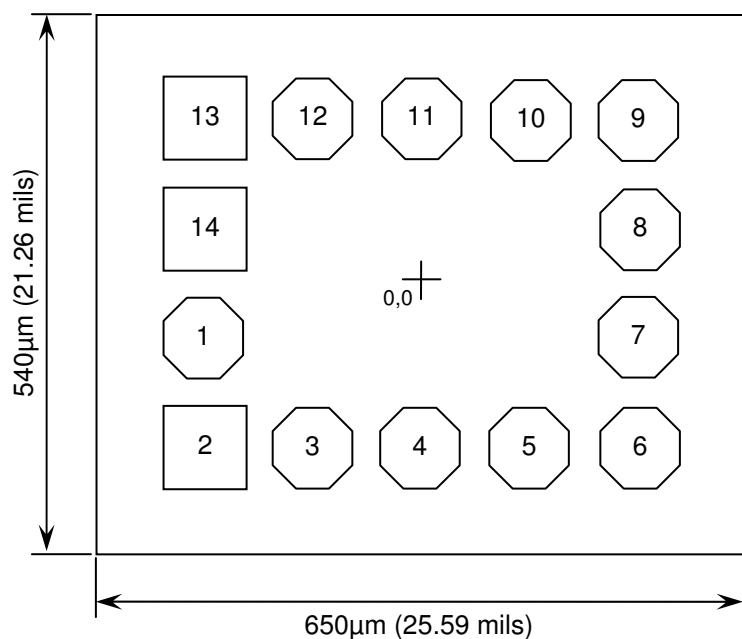




High Speed CMOS TTL Input – 54HCT04

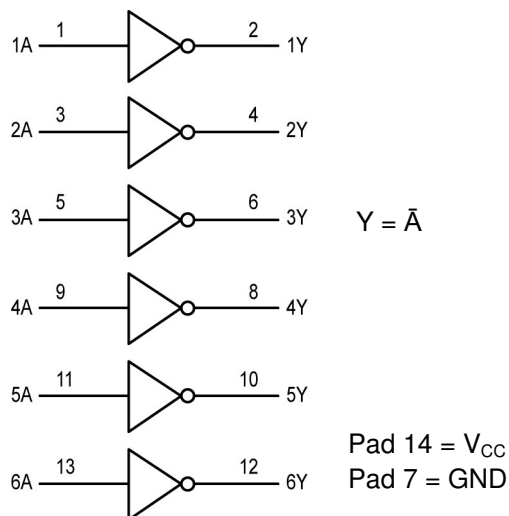
Rev 2.0
18/08/25

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	1A	-220	-55
2	1Y	-220	-165
3	2A	-110	-165
4	2Y	0	-165
5	3A	110	-165
6	3Y	220	-165
7	GND	220	-55
8	4Y	220	55
9	4A	220	165
10	5Y	110	165
11	5A	0	165
12	6Y	-110	165
13	6A	-220	165
14	V _{CC}	-220	55
CONNECT CHIP BACK TO V _{CC} OR FLOAT			

Logic Diagram



Function Table

INPUTS		OUTPUT	
A		Y	
H		L	
L		H	
H = High level (steady state)			
L = Low level (steady state)			





High Speed CMOS TTL Input – 54HCT04

Rev 2.0

18/08/25

Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC Input Current	I_{IN}	± 20	mA
DC Output Current, per pad	I_{OUT}	± 25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	± 50	mA
Power Dissipation in Still Air ²	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature Range	T_J	-55	+125	°C
Input Rise or Fall Times	t_r, t_f	-	500	ns

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Minimum High-Level Input Voltage	V_{IH}	4.5V	$V_{OUT} = 0.1V$ $ I_{OUT} \leq 20\mu A$	2.0	2.0	2.0	V
		5.5V		2.0	2.0	2.0	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	$V_{OUT} = V_{CC} - 0.1V$ $ I_{OUT} \leq 20\mu A$	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	V_{OH}	4.5V	$V_{IN} = V_{IL}$ $ I_{OUT} \leq 20\mu A$	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	$V_{IN} = V_{IL}$ $ I_{OUT} \leq 4.0mA$	3.98	3.84	3.70	
Maximum Low-Level Output Voltage	V_{OL}	4.5V	$V_{IN} = V_{IH}$ $ I_{OUT} \leq 20\mu A$	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IH}$ $ I_{OUT} \leq 4.0mA$	0.26	0.33	0.40	

4. -55°C $\leq T_J \leq$ +125°C





High Speed CMOS TTL Input – 54HCT04

Rev 2.0

18/08/25

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Maximum Input Leakage Current	I _{IN}	5.5V	V _{IN} = V _{CC} or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current ³	I _{CC}	5.5V	V _{IN} = V _{CC} or GND I _{OUT} = 0μA	1	10	40	μA
Additional Quiescent Supply Current ⁵	ΔI _{CC}	5.5V	V _{IN} = 2.4V, Any One Input. V _{IN} = V _{CC} or GND, Other Inputs I _{OUT} = 0μA	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

5. Total Supply Current = I_{CC} + ΣΔI_{CC}.

AC Electrical Characteristics⁶

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Maximum Propagation Delay, Input A to Input Y (Figure 1,2)	t _{PLH}	5V ±10%	C _L = 50pF, t _r = t _f = 6ns	15	19	22	ns
Maximum Propagation Delay, Input A to Input Y (Figure 1,2)	t _{PHL}	5V ±10%	C _L = 50pF, t _r = t _f = 6ns	17	21	26	
Maximum Output Rise and Fall Time (Figure 1,2)	t _{TLH} , t _{THL}	5V ±10%	C _L = 50pF, t _r = t _f = 6ns	15	19	22	ns
Maximum Input Capacitance	C _{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate ⁷	C _{PD}	-	T _J = 25°C, V _{CC} =5.0V	TYPICAL			pF
				22			

6. Not production tested in die form, characterized by chip design and tested in package.

7. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

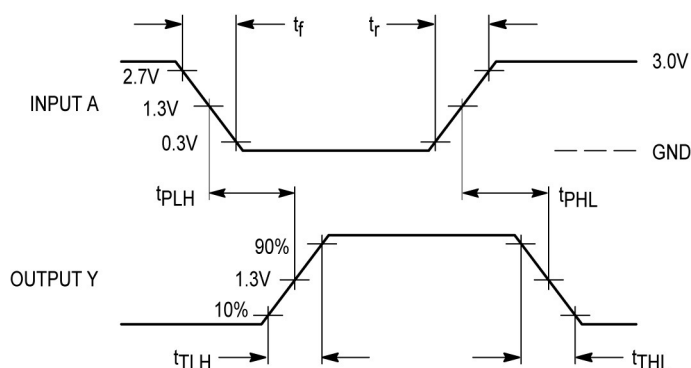




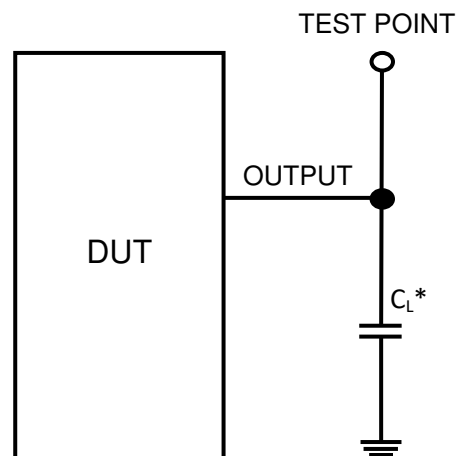
High Speed CMOS TTL Input – 54HCT04

Rev 2.0
18/08/25

Switching Waveform



Test Circuit



* Includes all probe and jig capacitance

Figure 1 – Propagation Delay & Output Transition Time

Figure 2

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

